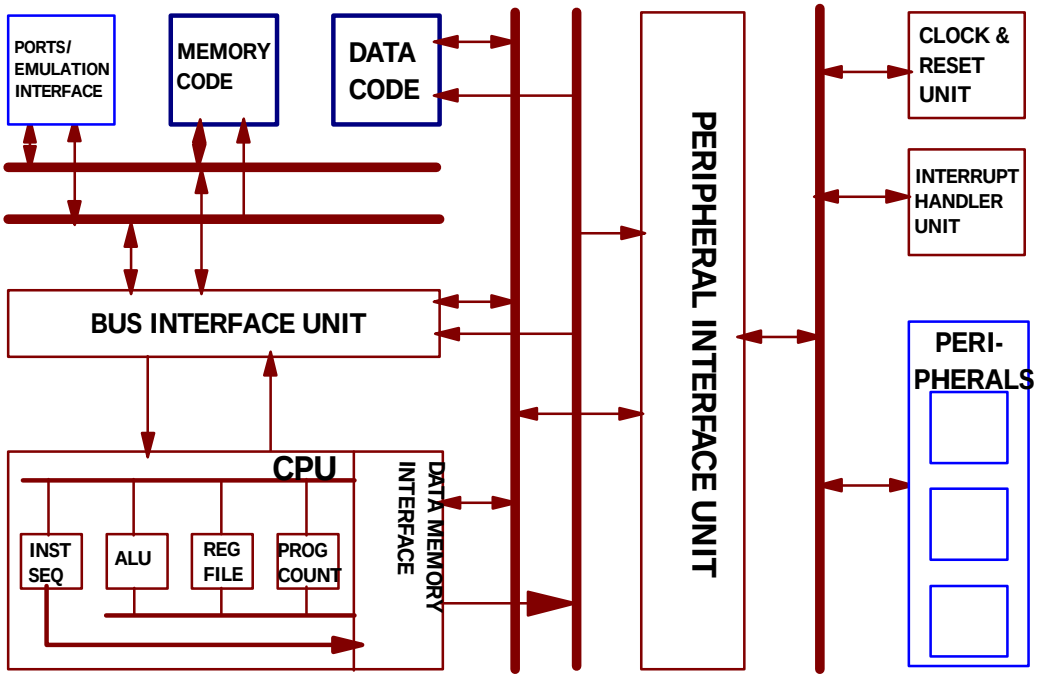
C 251 CPU Basic Features

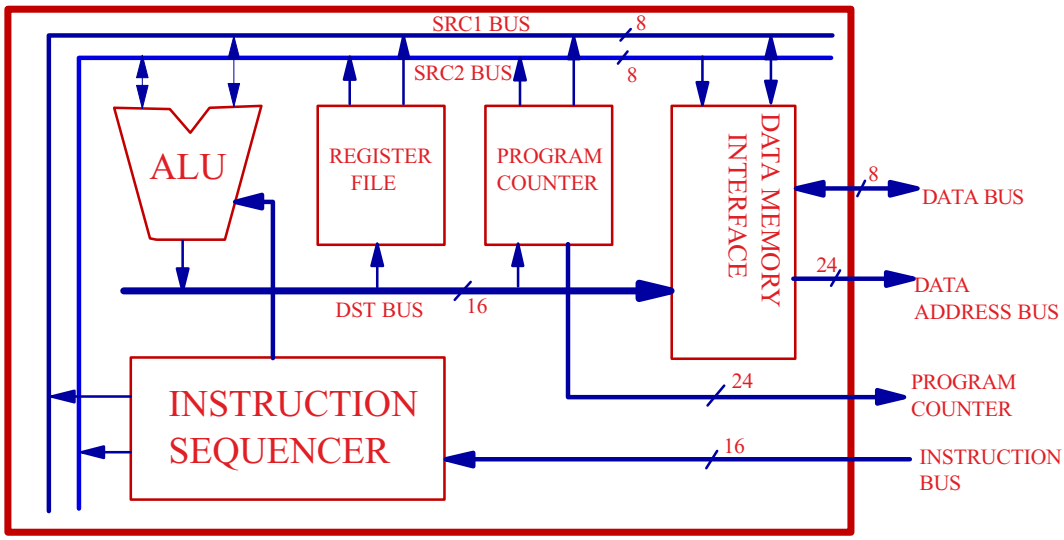
Internal Architecture

- C 251 CPU Is The Core Of The C 251 Product Family
  - ALU
  - Instruction Sequencer
  - Program Counter
  - Register File
  - High speed source & destination buses
- 8-Bit Internal Micro-Code
  - Fast : 2 clock-periods per state compared to 12 for the C51
- Three Stages Of Pipeline
  - Instruction Fetch & Decode
  - Address generation & data fetch
  - Execution & Write
- Register File
  - 32 bytes of registers
  - R0-R7 (4 Banks)
  - Data Pointer (DPX), Stack Pointer (STX)
- CPU Interfaces
  - 16-bit instruction bus (2 bytes/state code fetch)
  - 8-bit data bus (1 byte/state data transfer)

Product Architecture



C 251 CPU



C 251 Address Space

- General Features
  - One contiguous 16 megabyte address space for code & data
  - Same address space for internal & external access
  - Some addresses already allocated for data registers and SFR

- Code Memory
  - Located anywhere in the address space (except reserved locations)
  - Reset address located in the lowest byte of C51 program memory

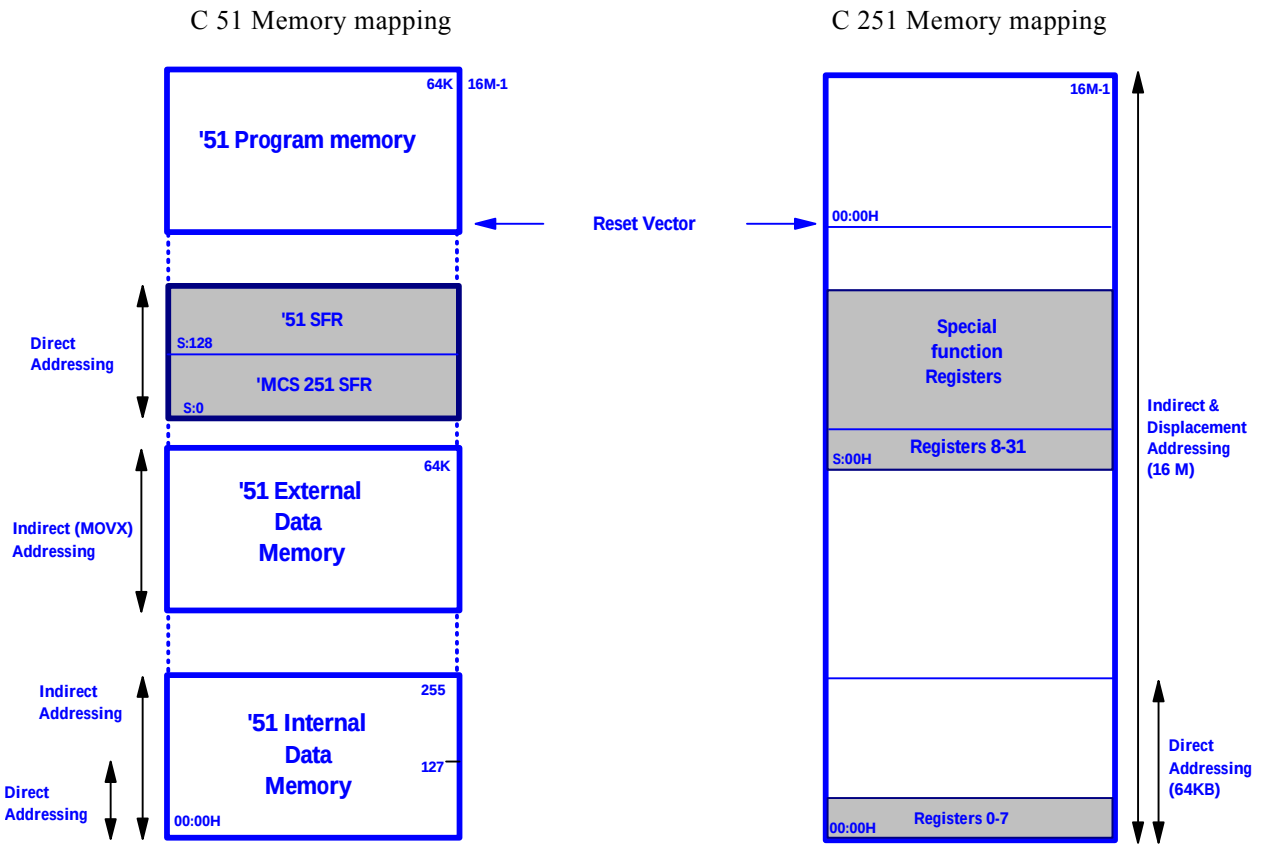
- Data Memory
  - Located anywhere in the address space (except reserved locations)
  - First 32 bytes in CPU (register file) are general purpose registers & data memory
  - Application related on-chip data memory
  - C51 external data memory mapped in the 16 Mbyte address range

- Register File
  - First 32 bytes mapped between 00-1fh to support C51 register banking
  - Registers 0-15 can be addressed by byte, word or double word
  - Upper registers can be addressed by word or double word

- SFR
  - SFRs are mapped like the data memory
  - SFRs provide status information of an on-chip peripheral

- Stack Pointer
  - Stack pointer is located at address 30h
  - Enhanced stack access through a rich set of addressing modes

C 251 Address Space



Instruction Set

- General Features
  - Powerful C 251-specific instructions
  - All C51 instructions are available
  - Configuration as C 251 or C51 during reset
  - Use of C 251 instruction in C 51 mode by escape code and vice-versa
  - C 251 instructions operate on 8 or 16 bit operands
  - "C" language programming efficiency
  - Data - , bit- and control instructions

- Addressing Modes
  - Register addressing : the instruction specifies the register which contains the operand.
  - Immediate addressing : the instruction contains the operand.
  - Direct addressing : the instruction contains the operand address.
  - Indirect addressing : the instruction specifies the register containing operand address.
  - Displacement addressing : the sum of the register and a signed offset specified by the instruction is the operand address.
  - Relative addressing : the instruction contains the relative offset from the next instruction to target address.
  - Bit addressing : the instruction contains the bit address.

Instruction Set Table

8/16 bit instructions		bit instructions		control instructions	
mnemonic	description	mnemonic	description	mnemonic	description
ADD	add	CLR	clear	JE	Jump if
SUB	substract	SETB	set bit	JNE	condition
CMP	compare	CPL	complement bit	JL...	
INC	increment	ANL	logical AND bit		
DEC	decrement	ANL/	log AND bit inv.	JB	jump if bit..
MUL	multiply*	ORL	logical OR bit	JNB...	
DIV	divide*	ORL/	log OR bit inv.		
ANL	logical AND	MOV	move	NOP	no instruction
ORL	logical OR			SJMP	short jump
XRL	logical XOR			LJMP	long jump
SLL	shift left logical			EJMP	extended jump
SRL	shift right logic.				
SRA	shift			LCALL	long call
MOV	move			ECALL	extended call
PUSH	push			TRAP	trap
POP	pop			RET	return

Interrupts

- General Features
  - 64 Interrupts
  - 1 non-maskable interrupt (second priority)
  - 1 trap instruction interrupt (first priority)
  - 62 maskable interrupt sources
  - 4 interrupt priority levels

- Interrupt Latency
  - Worst case latency time = longest instruction time + arbitration & transfer
  - Arbitration & transfer time = 8 states
  - Worst case latency time (16 bit DIV instruction) = 29 states
  - Worst case latency time without 16bit DIV inst. = 19 states (16 bit mul inst.)
    (corresponding to 1.9us with 20 MHz crystal frequency)

C 51 Compatibility

- C 251 Executes Both C 251 instructions and all C51 instructions

- Timing Issues
  - Minimum direct improvement vs. C51 microcontroller is about 5 times (up to 15times)
  - Examples Of Speed-Up :
  - C 251/C51 speed ratio for an 8 bit data instruction

Mul	:	4.8
DIV	:	2.4
ANL/ORL	:	12.0

Emulation Tools

- Improved On Chip "Hook" system
  - No special emulation circuit needed
  - Emulation at full processor speed
  - Full circuit simulation
  - "C"-compiler